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WHAT IS CLAIMED IS:

1.   A system for determining a bit error rate of bits in a
digital communication system, comprising:

5   - a transmitting station;

                          - a receiving station having a decoder (102);

                          - the transmitting station arranged for transmitting a bit
sequence to a receiving station;

                          - the receiving station arranged for receiving the bit
10   sequence (S1);

                          - the decoder (102) arranged for decoding one or more bits
out of the received bit sequence;

                          - a plurality of look-up tables (104, 105) arranged for
containing predetermined bit error rates related to ranges of soft output
15   values;
        characterised in that the system further comprises:

                          - a quantizer (103) being arranged for quantizing the
received bit (S2);

                          - a switch (106) being arranged for selecting an output
20   (S7, S8) representing a Bit error Rate contribution, of one of the look
up tables (104, 105) out of the plurality of look up tables, the
selection being based on the quantized bit (S6);

                          - a soft-output (S5) of the decoder (102) being arranged as
an index to the plurality of look up tables (104, 105) for retrieving a
25   bit error rate contribution to the bit error rate of a received bit
sequence;

                          - a summing and scaling device (107) being arranged for
accumulating and averaging the bit-wise BER (S9).

2.   The system as claimed in claim 1, wherein the lookup tables
30   (104, 105) are replaced by one or more processing devices, arranged for
providing accompanying values for the Bit Error Rate contribution (S7,

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S8) on input of the value of the soft output (S5).

3.   The system as claimed in claim 2, wherein the processing device is a floating point processor.

4.   The system as claimed in claim 1, wherein the decoder is a turbo-decoder.

5.   The system as claimed in claim 1, wherein the decoding algorithm is the Maximum A Posteriori algorithm (MAP).

6.   The system as claimed in claim 1, wherein the decoding algorithm is the Logarithmic Maximum A Posteriori algorithm (LOG-MAP).

7.   The system as claimed in claim 1, wherein the decoding algorithm is the Maximum-Logarithmic-Maximum A Posteriori algorithm (MAX-LOG-MAP).

8.   The system as claimed in claim 1, wherein the decoding algorithm is the Soft Output Viterbi Algorithm (SOVA).

9.   A receiving station system arranged for determining a bit error rate of bits in transmitted bit sequence, comprising:

        - a decoder (102) arranged for decoding one or more bits out of the received bit sequence;

        - a plurality of look-up tables (104, 105) arranged for containing predetermined bit error rates related to ranges of soft output values;

characterised in that the system further comprises:

        - a quantizer (103) being arranged for quantizing the received bit (S2);

        - a switch (106) being arranged for selecting an output (S7, S8) representing a Bit Error Rate contribution, of one of the look up tables (104, 105) out of the a plurality of look up tables, the selection being based on the quantized bit (S6);

        - a soft-output (S5) of the decoder (102) being arranged as an index to the plurality of look up tables (104, 105) for retrieving a bit error rate contribution to the bit error rate of a received bit

sequence;

       - a summing and scaling device (107) being arranged for accumulating and averaging the bit-wise BER (S9).

10.   The receiving station system as claimed in claim 9, wherein the receiving station system is a mobile unit within a wireless communication system.

11.   The receiving station system as claimed in claim 9, wherein the receiving station is a radio base station within a CDMA communication system.

12.   The receiving station system as claimed in claims 9, 10 and 11, wherein the receiving station system operates in a wireless communication network according to a GSM, Bluetooth, or Code Division Multiple Access (CDMA) standard.

13.   A method for determining a bit error rate of bits in a digital communication system comprising a transmitting station and a receiving station having a decoder (102), comprising the steps of:

       - <u>transmitting</u> a bit sequence to the receiving station by the transmitting station;

       - <u>receiving</u> the bit sequence by the receiving station;

       - decoding a bit out of the received bit sequence by the decoder (102),

characterised in that the method further comprises the steps of:

       - <u>quantizing</u> the received bit (S2) by a quantizer (103);

       - <u>selecting</u> an output (S7, S8) of a look up table out of a plurality of look up tables (104, 105), by a switch (106), the selection being based on the quantized bit (S6);

       - <u>indexing</u> the selected look up table (104, 105), for obtaining a bit-wise bit error rate of the received bit sequence, by the soft-output (S5) of the decoder (102);

       - <u>accumulating and averaging</u> the bit-wise BER (S9) of the received bit sequence by a summing and scaling device (107), resulting in

the estimated average BER (S10).

14.   The method as claimed in claim 13, wherein the decoding method is turbo-decoding.

15.   The method as claimed in claim 13, wherein the decoding algorithm is the Maximum A Posteriori algorithm (MAP).

16.   The method as claimed in claim 13, wherein the decoding algorithm is the Logarithmic Maximum A Posteriori algorithm (LOG-MAP).

17.   The method as claimed in claim 13, wherein the decoding algorithm is the Maximum-Logarithmic-Maximum A Posteriori algorithm (MAX-LOG-MAP).

18.   The method as claimed in claim 13, wherein the decoding algorithm is the Soft Output Viterbi Algorithm (SOVA).